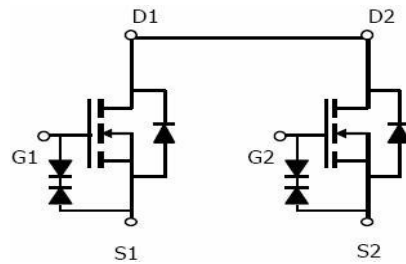


Dual N-Channel Enhancement Mode Power MOSFET

Description

The MXN3384 uses advanced trench technology design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. It is ESD protected



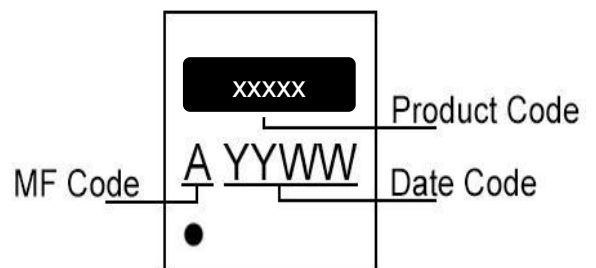
Schematic diagram

General Features

- ◆ $V_{DS} = 20V$, $I_D = 6A$
- ◆ @ $V_{GS} = 4.5V$ $R_{DS(ON)}$ (Typ.)=12.5m Ω
- ◆ @ $V_{GS} = 3.8V$ $R_{DS(ON)}$ (Typ.)=13m Ω
- ◆ @ $V_{GS} = 2.5V$ $R_{DS(ON)}$ (Typ.)=16.5m Ω

High density cell design for ultra low R_{dson}

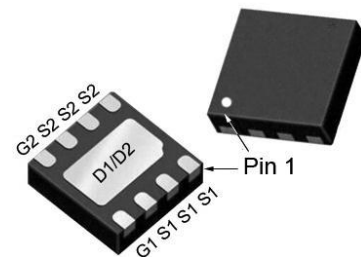
Fully characterized Avalanche voltage and current



Marking Description

Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



DFN3x3-8L top view

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	6	A
Drain Current-Pulsed (Note 1)	I_{DM}	36	A
Maximum Power Dissipation	P_D	2.5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	50	°C/W
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Electrical Characteristics (TA=25°C unless otherwise noted)

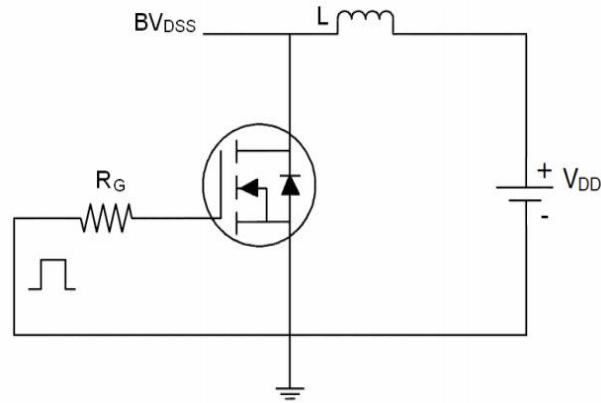
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	20	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V	-	-	1	μA
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±12V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 2)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.45	0.65	1.2	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =6A	-	12.5	17	mΩ
		V _{GS} =3.8V, I _D =6A	-	13	19	
		V _{GS} =2.5V, I _D =4A	-	16.5	24	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =10A	15	-	-	S
Dynamic Characteristics (Note 3)						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, F=1.0MHz	-	976	-	PF
Output Capacitance	C _{oss}		-	80	-	PF
Reverse Transfer Capacitance	C _{rss}		-	142	-	PF
Switching Characteristics (Note 3)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =10V, I _D =1A V _{GS} =10V, R _{GEN} =6Ω	-	7.2		nS
Turn-on Rise Time	t _r		-	12		nS
Turn-Off Delay Time	t _{d(off)}		-	22.8		nS
Turn-Off Fall Time	t _f		-	8.1		nS
Total Gate Charge	Q _g	V _{DS} =10V, I _D =6A, V _{GS} =4.5V	-	11		nC
Gate-Source Charge	Q _{gs}		-	2.6	-	nC
Gate-Drain Charge	Q _{gd}		-	3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 2)	V _{SD}	V _{GS} =0V, I _S =1A	-	-	1.2	V
Diode Forward Current (Note 1)	I _S		-	-	3.5	A

Notes:

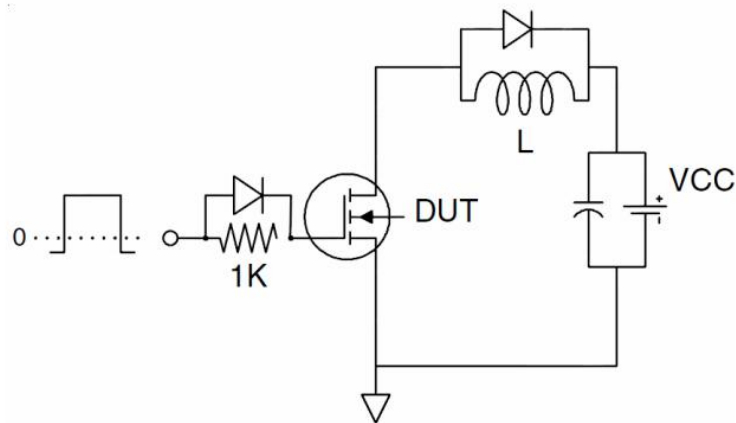
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Test Circuit

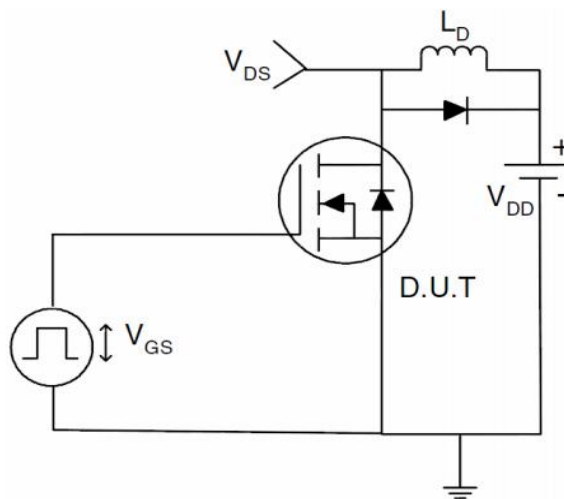
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

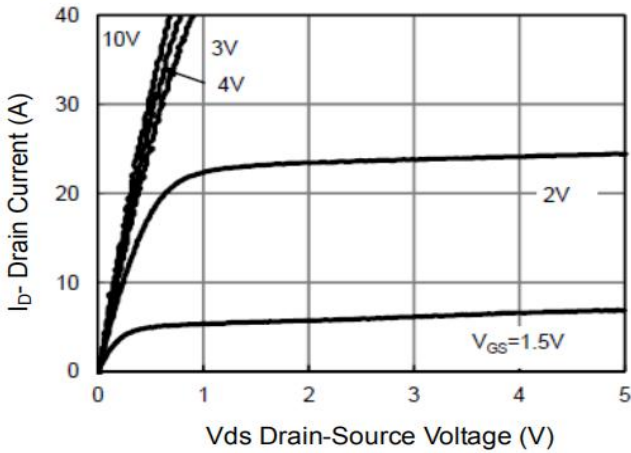


Figure 1 Output Characteristics

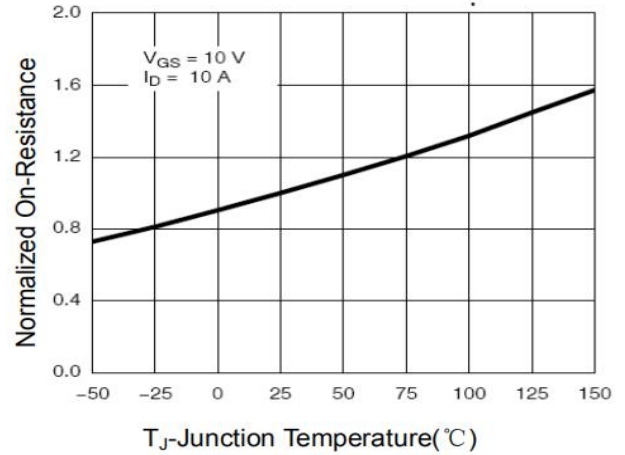


Figure 4 Rdson-Junction Temperature

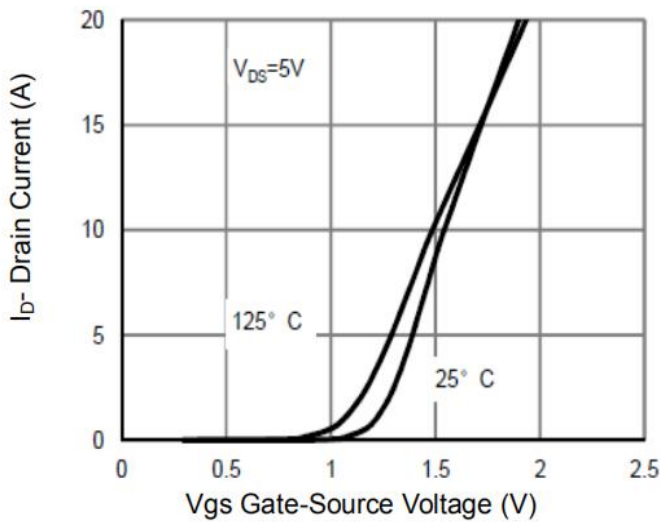


Figure 2 Transfer Characteristics

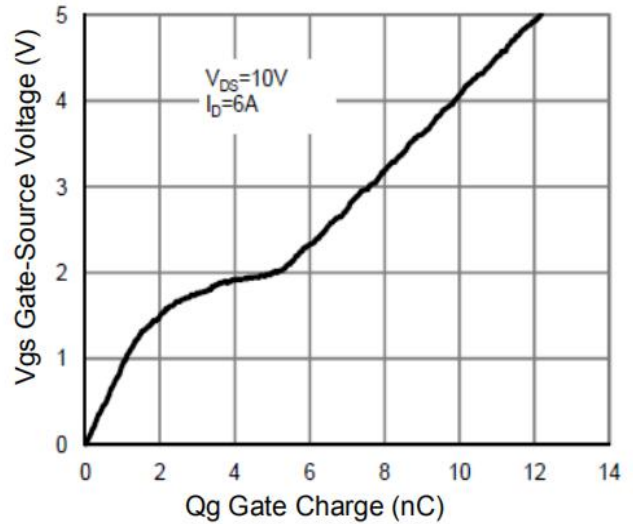


Figure 5 Gate Charge

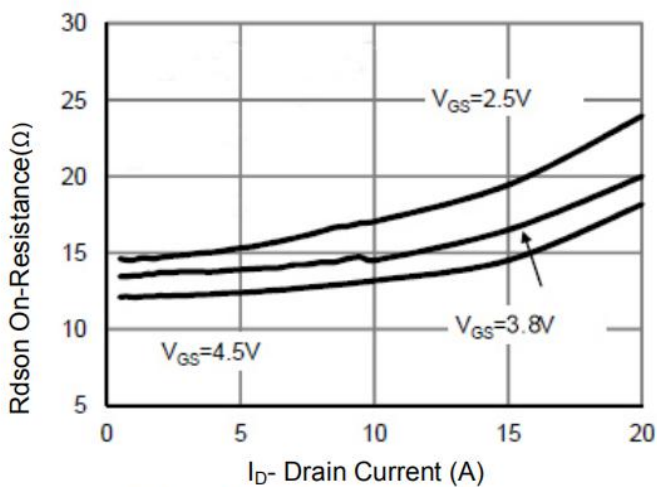


Figure 3 Rdson- Drain Current

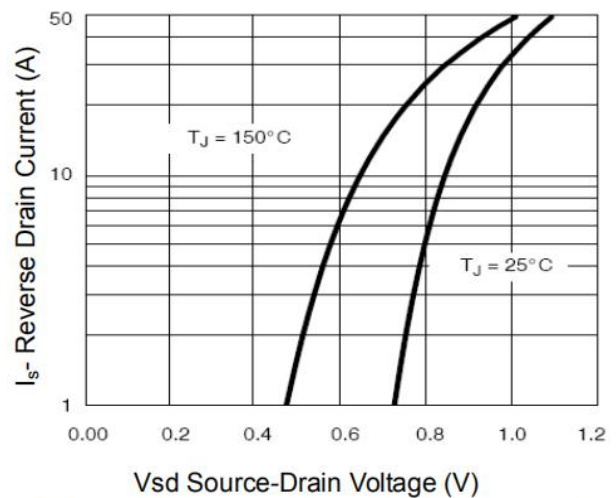


Figure 6 Source- Drain Diode Forward

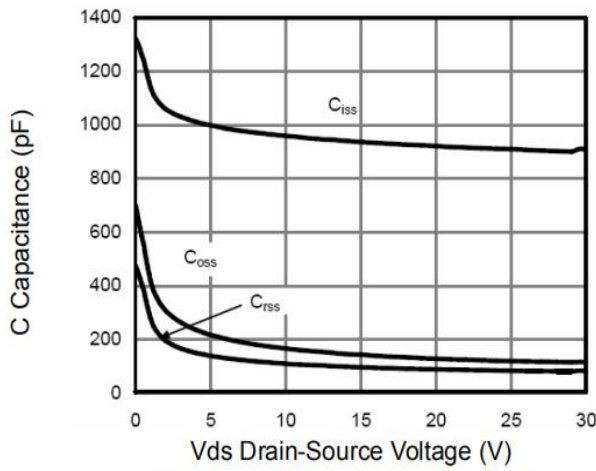


Figure 7 Capacitance vs Vds

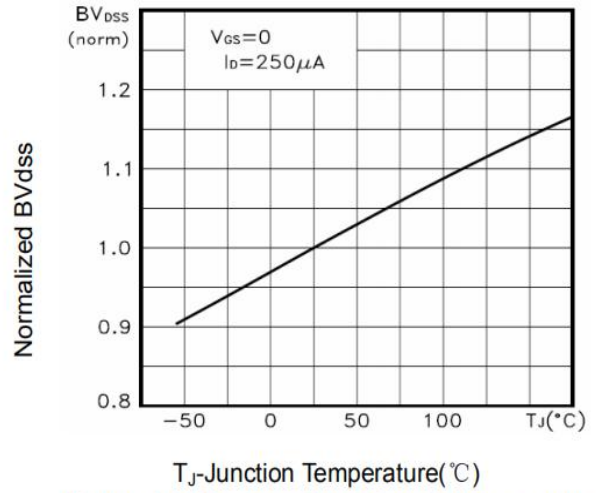


Figure 9 BV_{DSS} vs Junction Temperature

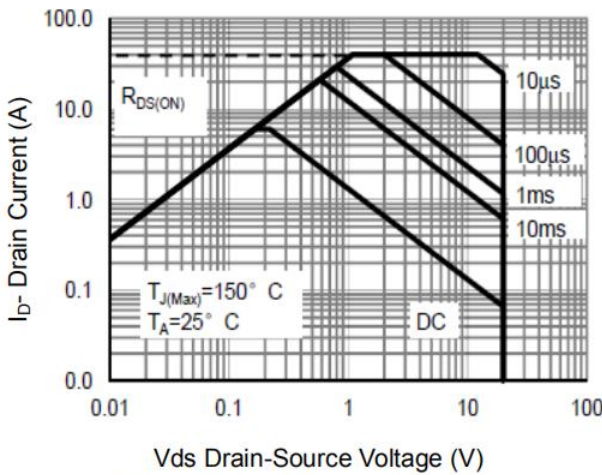


Figure 8 Safe Operation Area

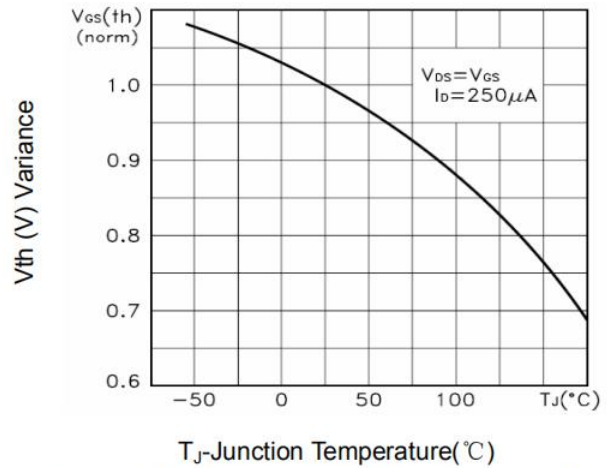


Figure 10 V_{GS(th)} vs Junction Temperature

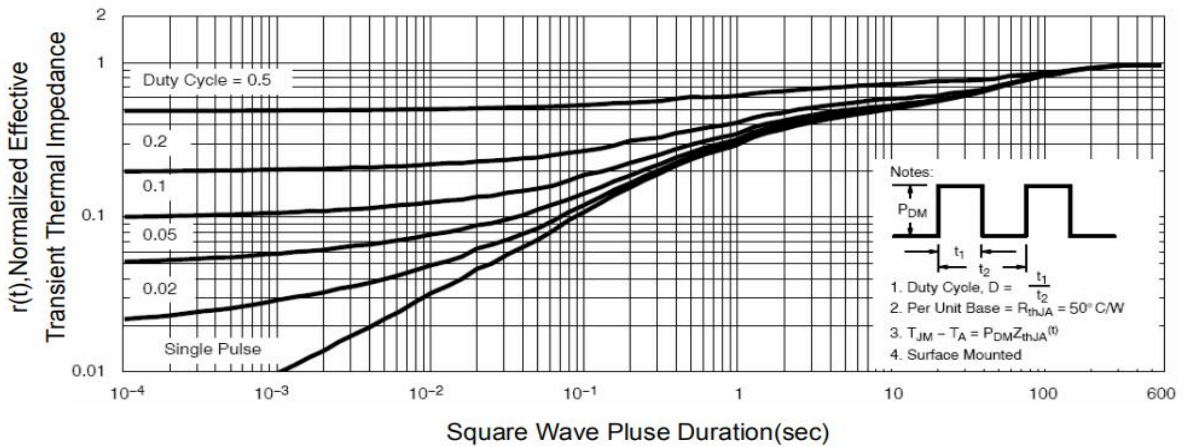


Figure 11 Normalized Maximum Transient Thermal Impedance

Package Dimension
DFN 3x3 MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	0.7		0.8	I		0.203	
B	0.25		0.35	J	2.2		2.4
C	0.2			K	1.4		1.6
D	2.924		3.076				
E	2.924		3.076				
F	0.324		0.476				
G		0.65					
H	0		0.05				

