

## N-Channel Enhancement Mode Power MOSFET

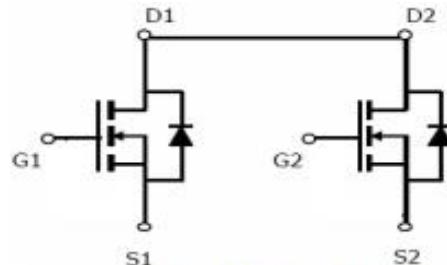
The MX8806B uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications.

### General Features

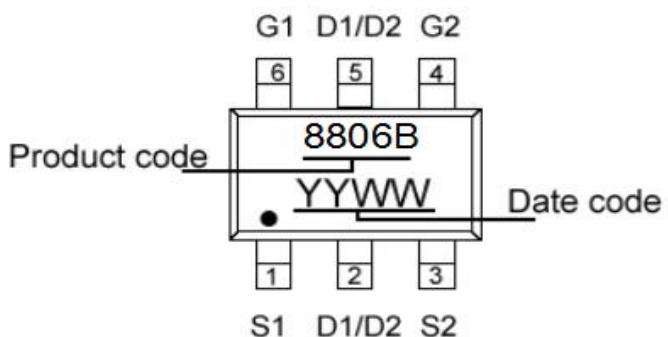
- ◆  $V_{DS} = 15V, I_D = 6A$
- $R_{DS(ON)} < 15m\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} < 17m\Omega @ V_{GS}=3.8V$
- $R_{DS(ON)} < 22m\Omega @ V_{GS}=2.5V$
- ◆ High Power and current handing capability
- ◆ Lead free product is acquired
- ◆ Surface Mount Package

### Applications

- ◆ PWM application
- ◆ Load switch



**Schematic diagram**



## Marking and pin assignment

SOT-23-6 (TOP VIEW)

### Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	15	V
Gate-Source Voltage	$V_{GS}$	$\pm 10$	V
Drain Current-Continuous	$I_D$	5	A
Drain Current-Pulsed (Note 1)	$I_{DM}$	20	A
Maximum Power Dissipation	$P_D$	1.5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	°C



MX8806B

## Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	R <sub>θJA</sub>	83.3	°C/W
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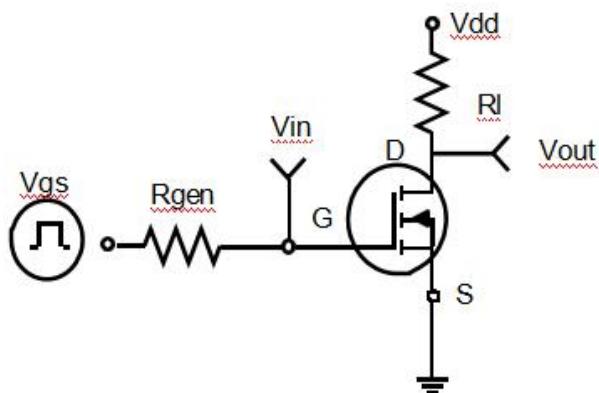
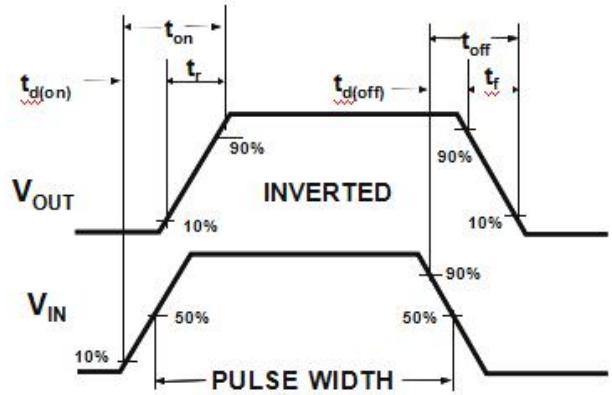
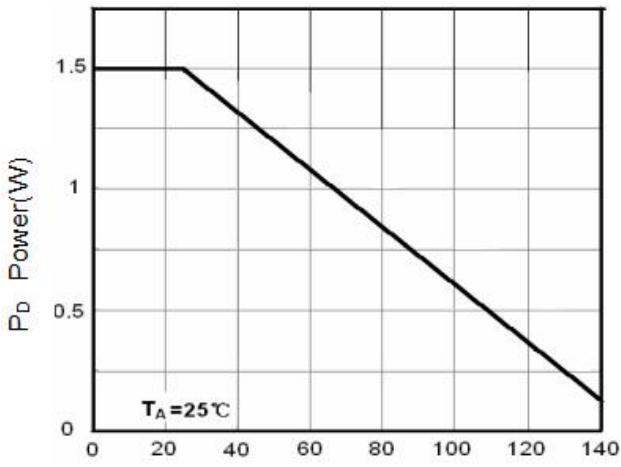
## Electrical Characteristics (TA=25°C unless otherwise noted)

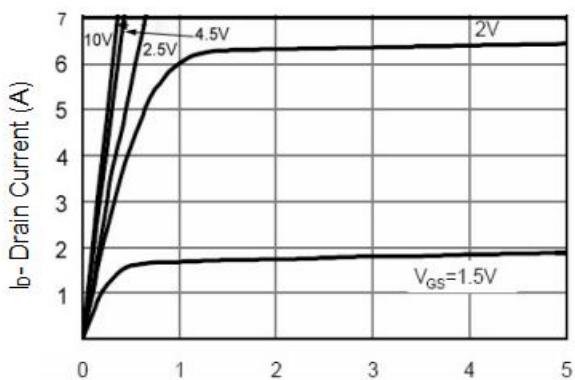
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	V <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	15	19	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.45	0.7	0.95	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =4.5A	10	12.8	15	mΩ
		V <sub>GS</sub> =3.8V, I <sub>D</sub> =4.0A	11	13.5	17	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =3.5A	15.5	18.6	22	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =5A	-	20	-	S
<b>Dynamic Characteristics (Note 4)</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, F=1.0MHz	-	1150	-	PF
Output Capacitance	C <sub>oss</sub>		-	185	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	145	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =10V, R <sub>L</sub> =1.35Ω V <sub>GS</sub> =5V, R <sub>GEN</sub> =3Ω	-	6		nS
Turn-on Rise Time	t <sub>r</sub>		-	13		nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	52		nS
Turn-Off Fall Time	t <sub>f</sub>		-	16		nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =5A, V <sub>GS</sub> =4.5V	-	15		nC
Gate-Source Charge	Q <sub>gs</sub>		-	0.8	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	3.2	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>s</sub> =1A	-	-	1.2	V
Diode Forward Current (Note 2)	I <sub>s</sub>		-	-	7	A

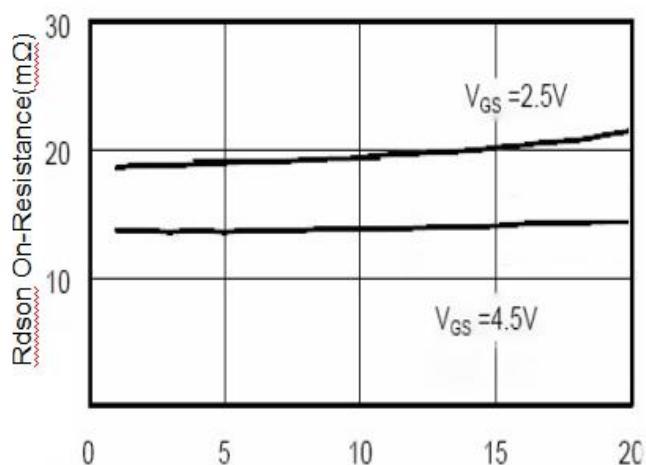
## Notes:

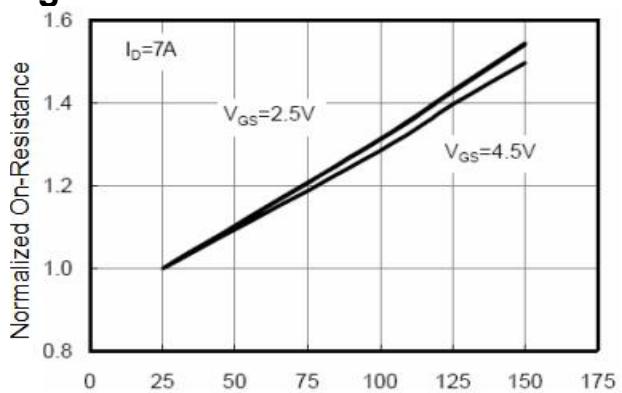
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.

Guaranteed by design, not subject to production

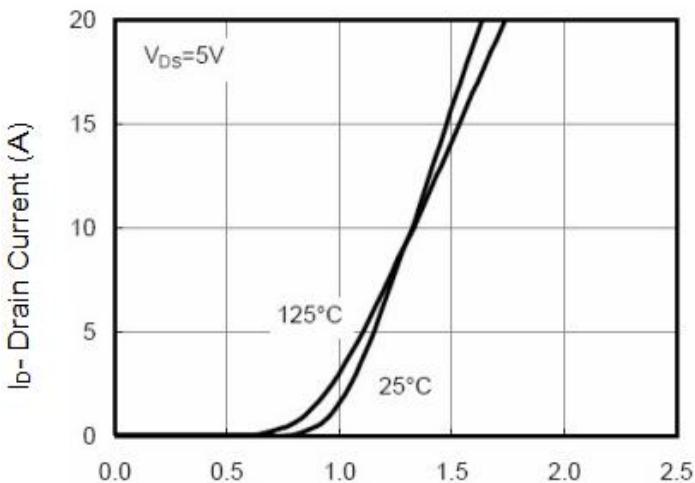
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

**Figure 1:Switching Test Circuit**

**Figure 2:Switching Waveforms**

 $T_J$ -Junction Temperature(°C)

**Figure 3 Power Dissipation**

 $V_{DS}$  Drain-Source Voltage (V)

**Figure 5 Output CHARACTERISTICS**

 $I_D$ - Drain Current (A)

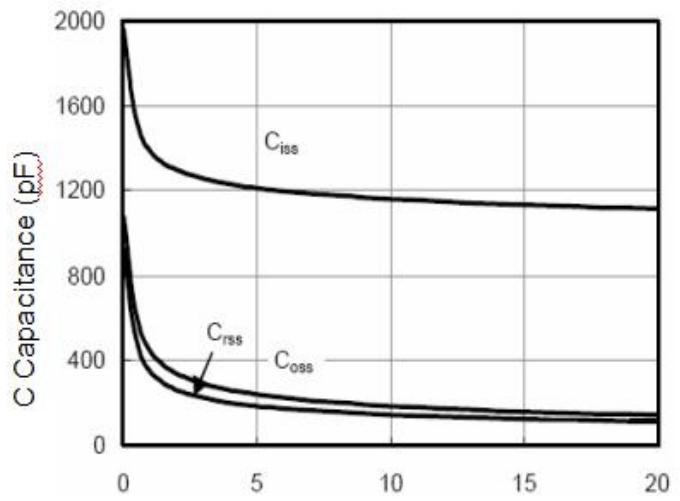
**Figure 4 Drain-Source On-Resistance**

 $T_J$ -Junction Temperature(°C)

**Figure 6 Drain-Source On-Resistance**



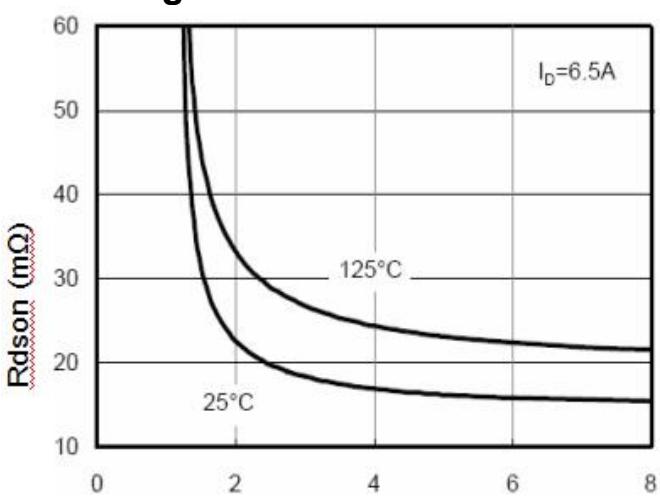
V<sub>GS</sub> Gate-Source Voltage (V)

**Figure 7 Transfer Characteristics**



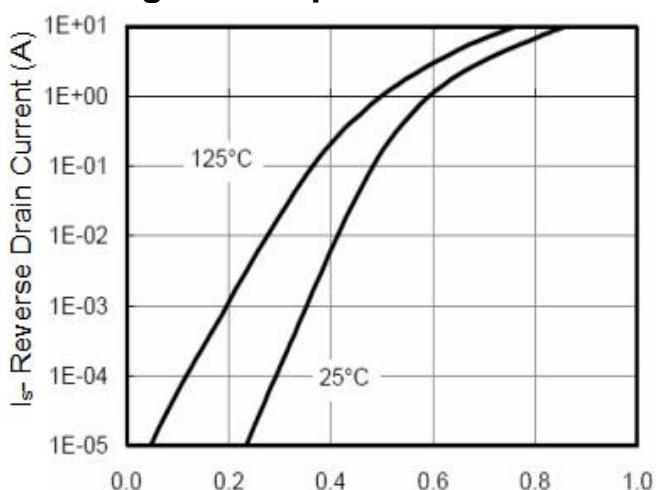
V<sub>DS</sub> Drain-Source Voltage (V)

**Figure 8 Capacitance vs V<sub>DS</sub>**



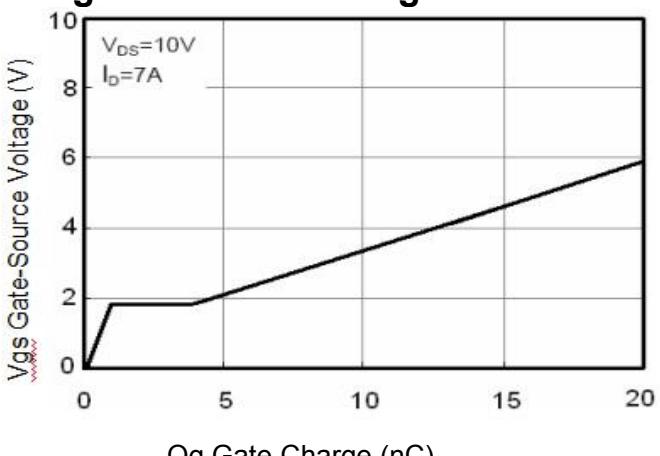
V<sub>GS</sub> Gate-Source Voltage (V)

**Figure 9  $R_{DS(on)}$  vs  $V_{GS}$**



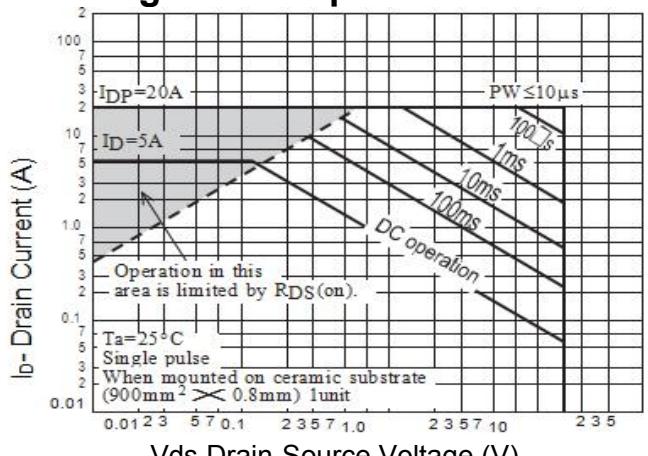
V<sub>DS</sub> Drain-Source Voltage (V)

**Figure 10 Capacitance vs  $V_{DS}$**

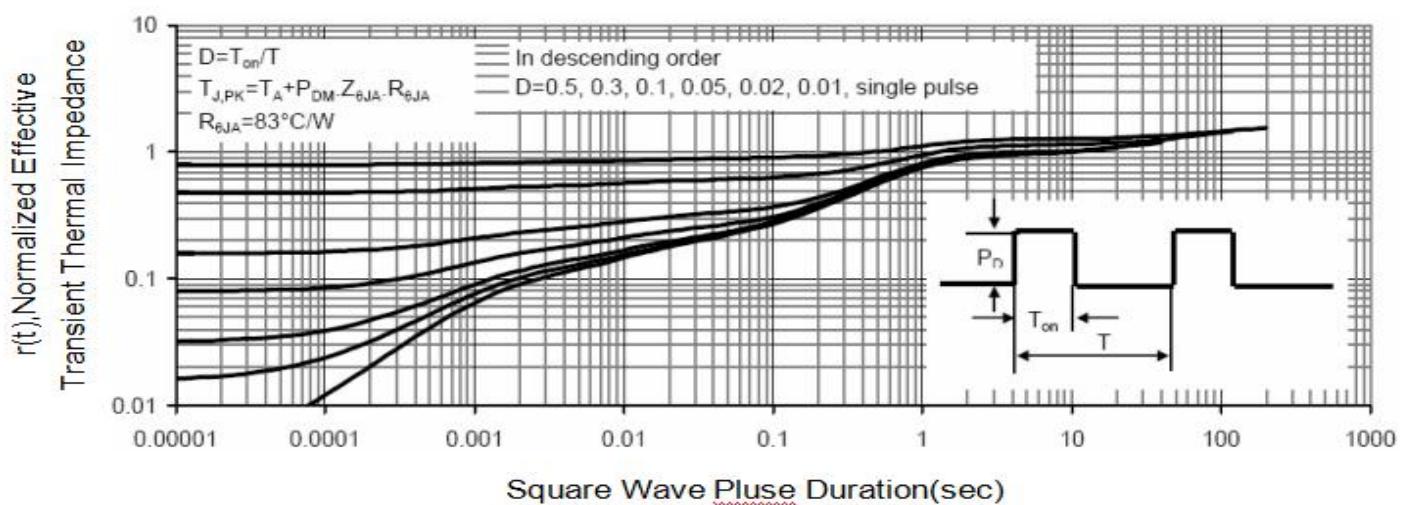


Q<sub>G</sub> Gate Charge (nC)

**Figure 11 Gate Charge**



**Figure 12 Safe Operation Area**



**Figure 13 Normalized Maximum Transient Thermal Impedance**

## SOT23-6 PACKAGE INFOR

