

## DESCRIPTION

The MXB03N08D uses advanced trench technology to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

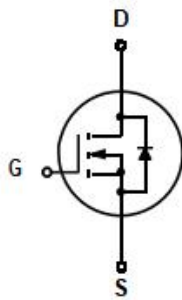
## GENERAL FEATURES

- $V_{DS}=80V$ ,  $I_D=200A$   
 $R_{DS(ON)}$ (Typ.)= $3.0m\Omega$  @  $V_{GS}=10V$
- Advanced trench cell design
- Surface-mounted package
- Trench MOS

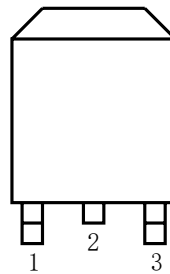
## APPLICATION

- BMS appliances
- High power inverter system
- Power appliances

## PINOUT



Schematic diagram



Top View TO-263

Pin	Description
1	Gate(G)
2	Drain(D)
3	Source(S)

## ORDERING INFORMATION

Part Number	Storage Temperature	Package	Devices Per Reel
MXB03N08D	-55°C to 150°C	TO-263	800

## ABSOLUTE MAXIMUM RATINGS ( $T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	80	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous ( $V_{GS}=10V$ ) <sup>(Note1)(Note3)</sup>	$I_D$	200	A
Pulsed Source Current <sup>(Note1)(Note2)(Note3)</sup>	$I_{DM}$	800	A
Diode Forward Current	$I_S$	200	A
Single Pulsed Avalanche Energy <sup>(Note1)</sup>	$E_{AS}$	1600	mJ
Total Power Dissipation <sup>(Note1)</sup>	$P_{tot}$	270	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	°C
Thermal Resistance, Junction-to-Case <sup>(Note1)</sup>	$R_{\theta JC}$	0.41	°C/W

Note 1. Surface Mounted on 1 in<sup>2</sup> pad area,  $t \leq 10$  sec

Note 2. Pulse width  $\leq 10 \mu s$ , duty cycle  $\leq 1\%$

Note 3. Limited by bonding wire



**ELECTRICAL CHARACTERISTICS** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
-----------	--------	------------	-----	-----	-----	------

**Off Characteristics**

Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_{DS}=250\mu A$	80	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=64V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA

**On Characteristics**

Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1.5	2.0	2.5	V
Drain-Source On-State Resistance <sup>(Note1)</sup>	$R_{DS(ON)}$	$V_{GS}=10V, I_{DS}=50A$	-	3.0	3.5	m $\Omega$

**Dynamic Characteristics<sup>(Note2)</sup>**

Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V, F=1.0MHz$	-	13200	-	pF
Output Capacitance	$C_{oss}$		-	950	-	pF
Reverse Transfer Capacitance	$C_{rss}$		-	810	-	pF

**Switching Characteristics<sup>(Note2)</sup>**

Turn-on Delay Time	$t_{d(on)}$	$V_{DS}=40V, I_{DS}=40A, V_{GEN}=10V, R_G=4.5\Omega, R_L=1\Omega,$	-	26	-	nS
Turn-on Rise Time	$t_r$		-	20	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	50	-	nS
Turn-Off Fall Time	$t_f$		-	18	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=64V, I_{DS}=80A, V_{GS}=10V$	-	257	-	nC
Gate-Source Charge	$Q_{gs}$		-	76	-	nC
Gate-Drain Charge	$Q_{gd}$		-	80	-	nC

**Drain-Source Diode Characteristics**

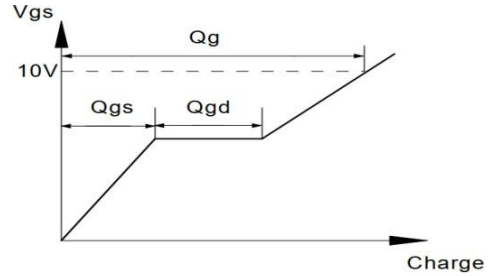
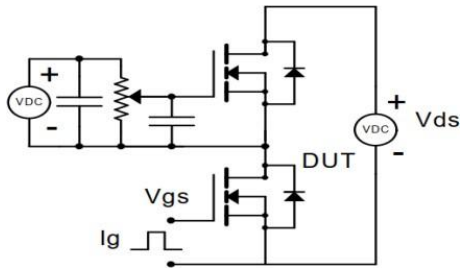
Diode Forward Voltage <sup>(Note1)</sup>	$V_{SD}$	$V_{GS}=0V, I_{SD}=30A$	-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$I_{SD}=30A, dl/dt=100A/\mu s$	-	65	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	83	-	nC

Note 1. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$

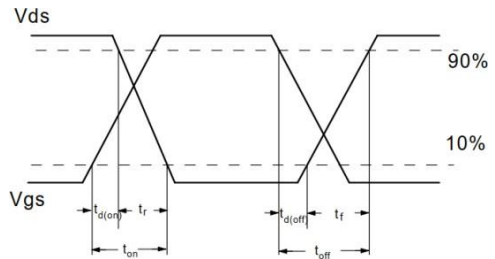
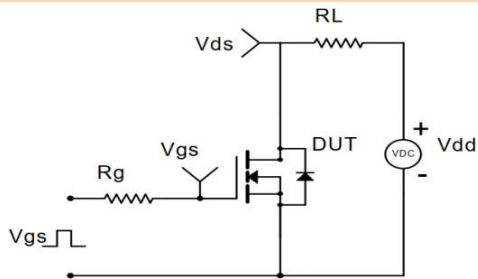
Note 2. Guaranteed by design, not subject to production testing

**TEST CIRCUIT AND WAVEFORM**

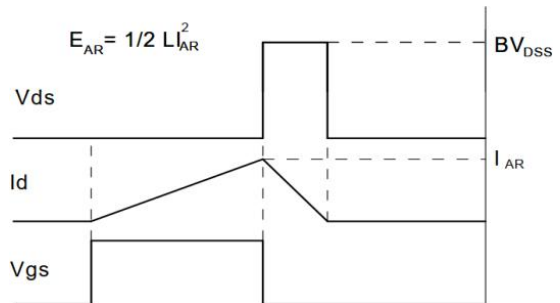
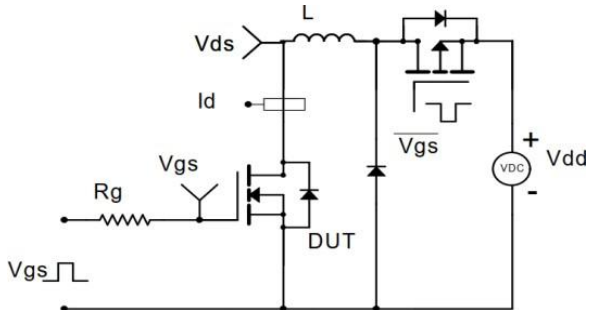
**1、 Gate Charge Test**



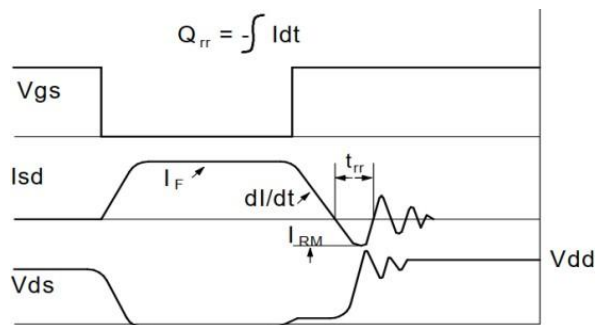
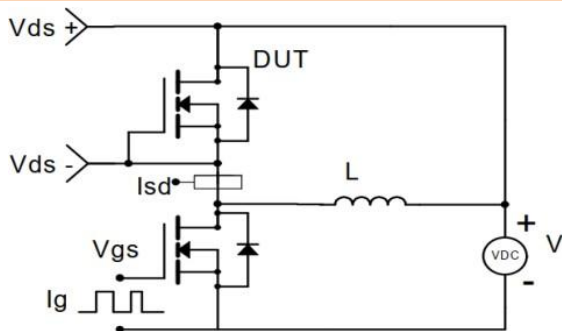
**2、 Resistive Switching Test**



**3、 Unclamped Inductive Switching (UIS) Test**

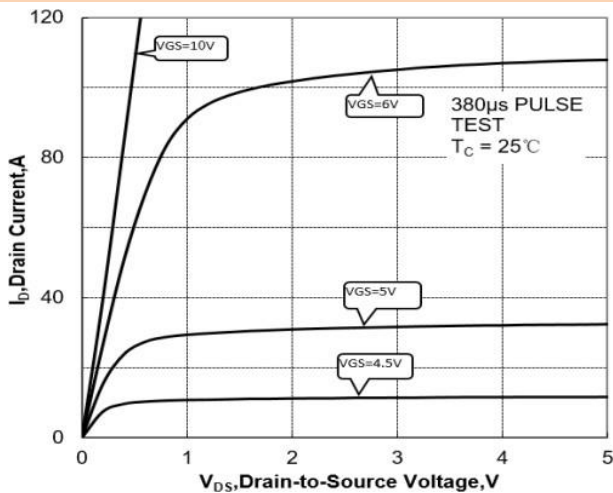


**4、 Diode Recovery Test**

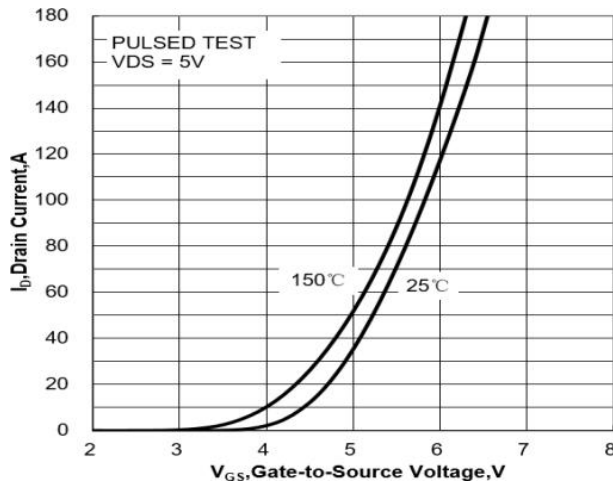


**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

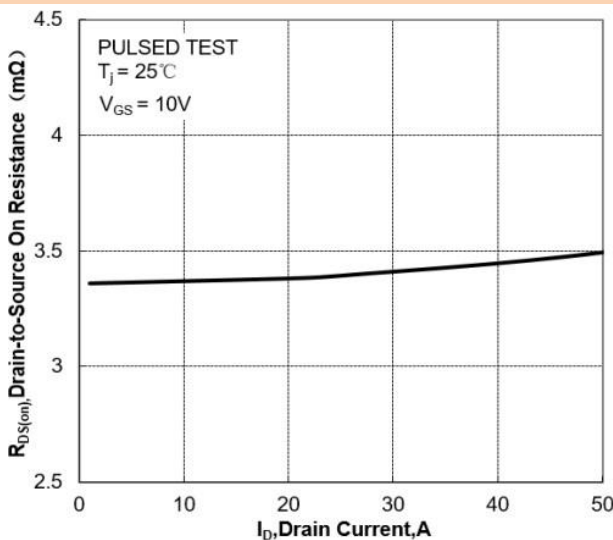
**Figure 1. Output Characteristics**



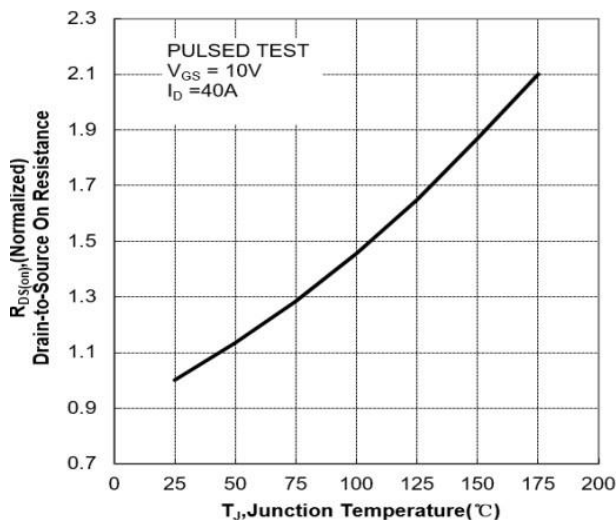
**Figure 2. Transfer Characteristics**



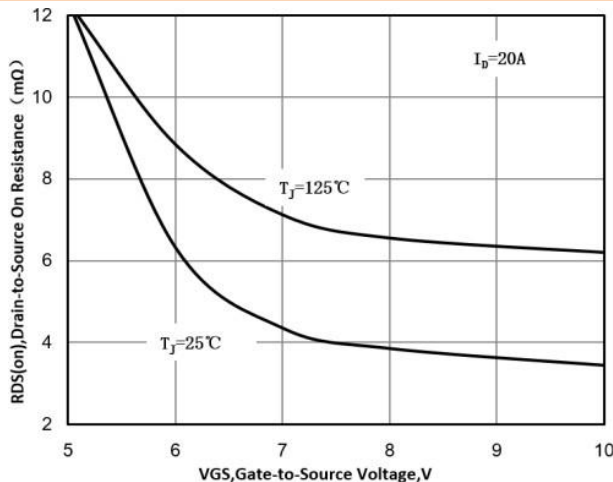
**Figure 3. On-Resistance vs. ID and VGS**



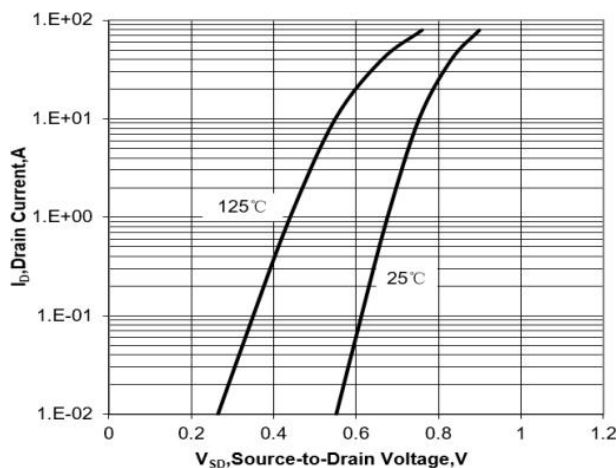
**Figure 4. On-Resistance vs. Junction Temperature**



**Figure 5. On-Resistance vs. VGS**



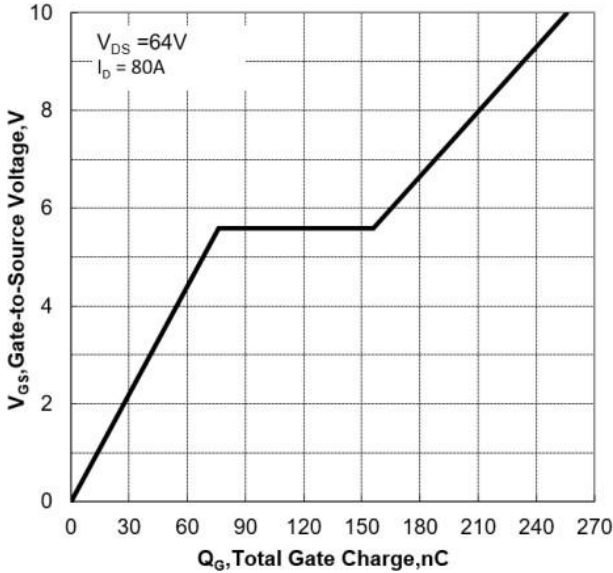
**Figure 6. Body Diode Forward Voltage**



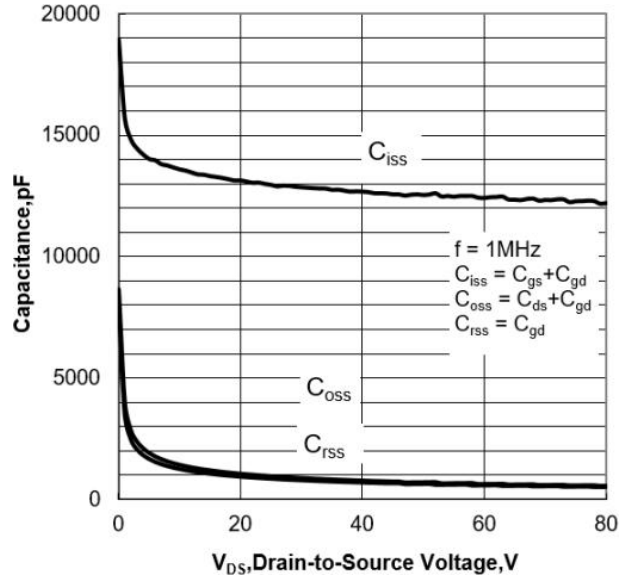


**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

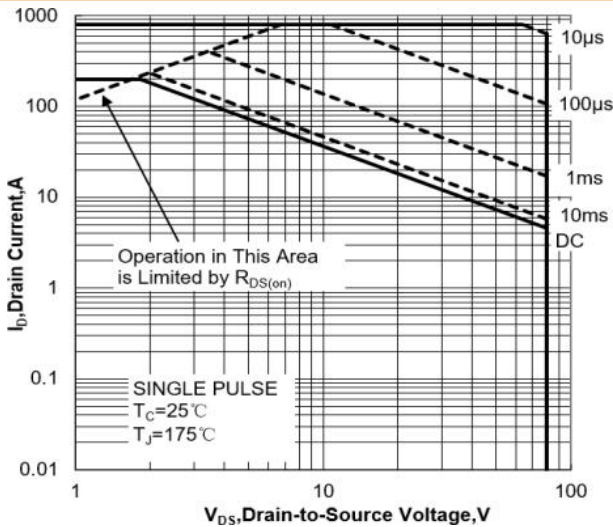
**Figure 7. Gate-Charge Characteristics**



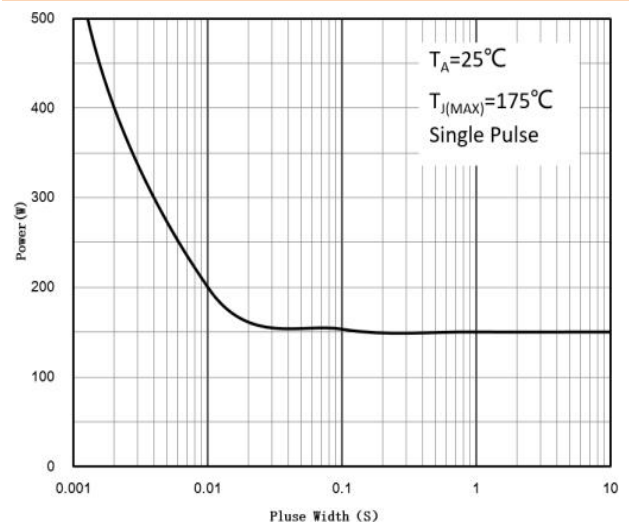
**Figure 8. Capacitance Characteristics**



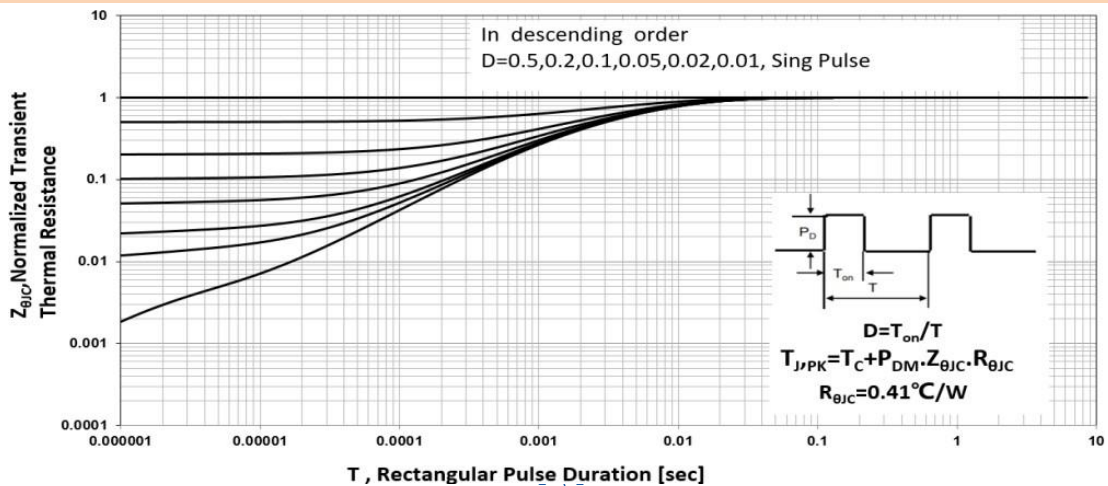
**Figure 9. Maximum Forward Biased Safe Operation Area**



**Figure 10. Single Pulse Power Rating Junction-to-Ambient**

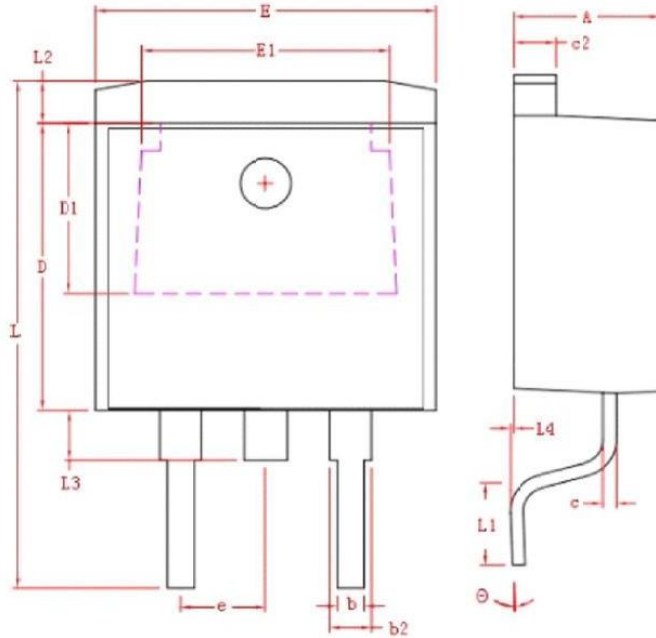


**Figure 11. Normalized Maximum Transient Thermal Impedance**



 **PACKAGE INFORMATION**

TO263-3L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	4.40	4.80
b	0.76	1.00
L4	0.00	0.25
C	0.36	0.50
L3	1.50 REF	
L1	2.29	2.79
E	9.80	10.40
E1	7.40 REF	
c2	1.25	1.45
b2	1.17	1.47
D	8.60	9.00
D1	5.10 REF	
e	2.54 REF	
L	14.6	15.8
θ	0° ± 3°	
L2	1.27 REF	