

DESCRIPTION

The MX15P03 uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

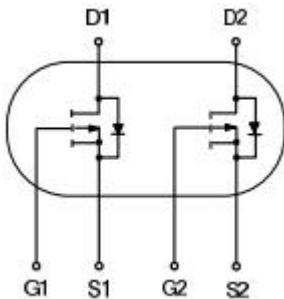
GENERAL FEATURES

- $V_{DS}=-30V$, $I_D=-10A$
- $R_{DS(ON)}(\text{Typ.})=24m\Omega$ @ $V_{GS}=-4.5V$
- $R_{DS(ON)}(\text{Typ.})=14.5m\Omega$ @ $V_{GS}=-10V$
- Low Thermal Resistance
- Advanced trench cell design

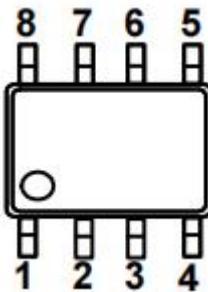
APPLICATION

- Motor drivers
- DC-DC Converter

PINOUT



Schematic diagram



SOP-8L top view

Pin	Description
1	Source(S1)
2	Gate(G1)
3	Source(S2)
4	Gate(G2)
5,6	Drain(D2)
7,8	Drain(D1)

ORDERING INFORMATION

Part Number	Storage Temperature	Package	Devices Per Reel
MX15P03	-55°C to 150°C	SOP8	3000

ABSOLUTE MAXIMUM RATINGS ($T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current($V_{GS}=-10V$) ^(Note1)	I_D	-10	A
Pulsed Source Current($V_{GS}=-10V$) ^{(Note1)(Note2)(Note3)}	I_{DM}	-60	A
Diode Forward Current	I_S	-10	A
Total Power Dissipation ^(Note1)	P_{tot}	20	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C
Thermal Resistance, Junction-to-Case ^(Note1)	$R_{\theta JC}$	6	°C/W

Note 1. Surface Mounted on 1 in² pad area, $t \leq 10$ sec

Note 2. Pulse width $\leq 10\mu s$, duty cycle $\leq 1\%$

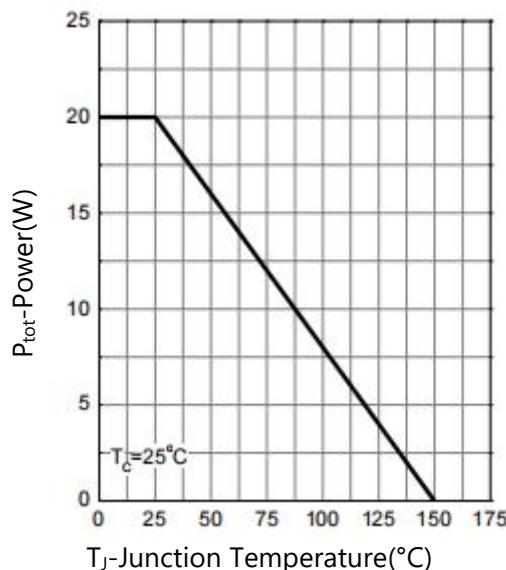
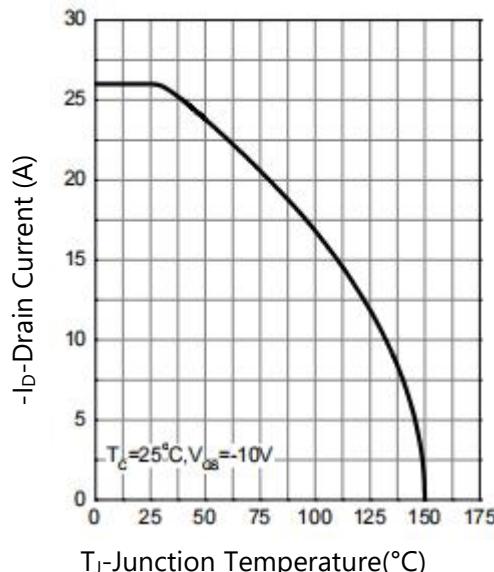
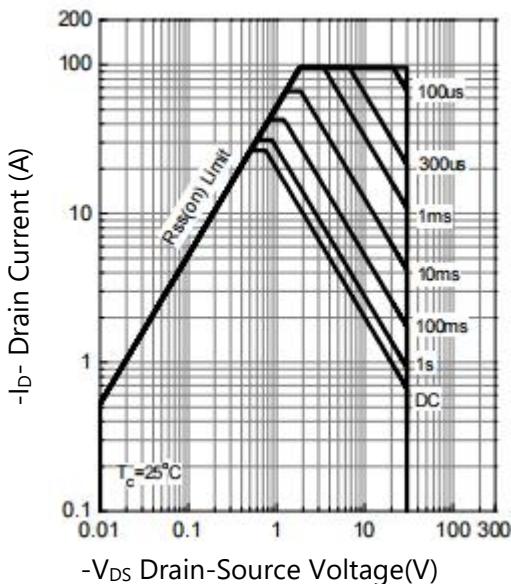
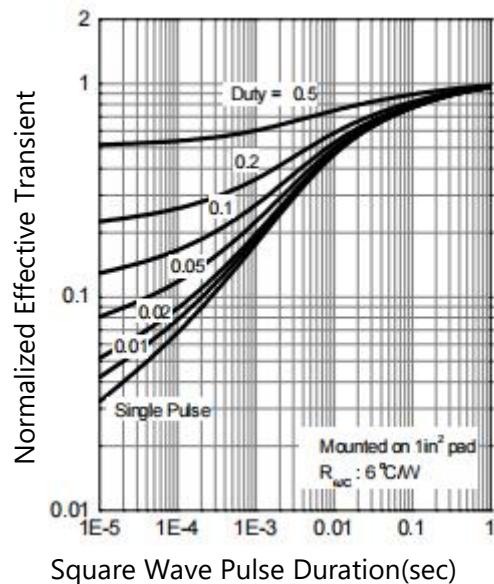
Note 3. limited by bonding wire

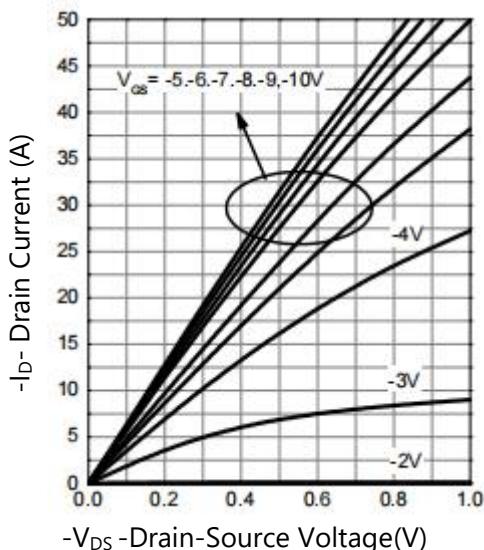
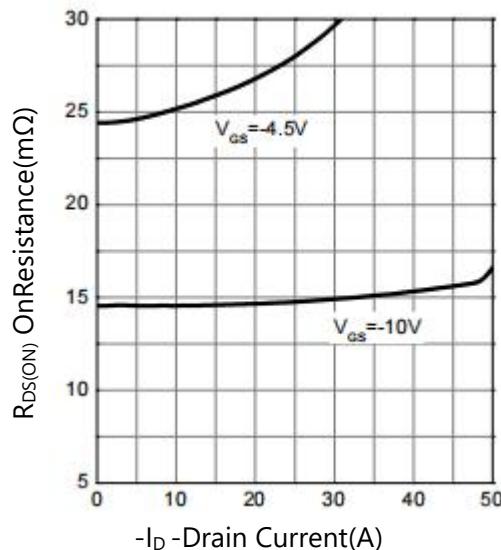
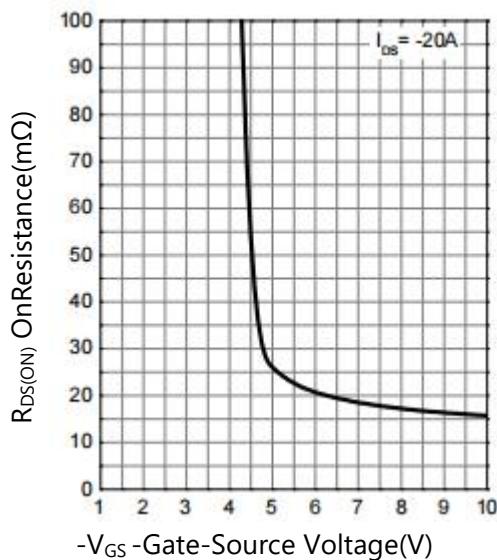
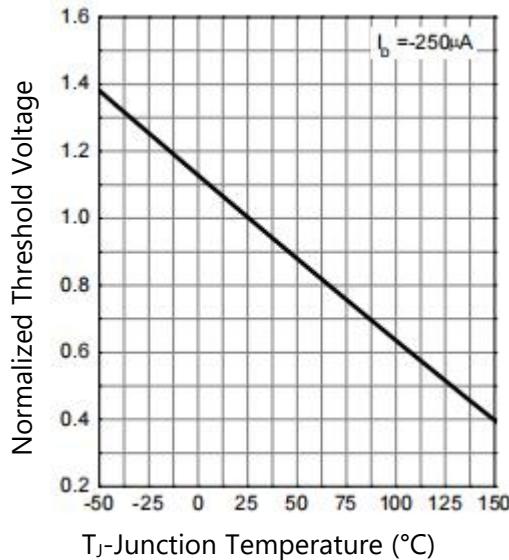

ELECTRICAL CHARACTERISTICS($T_C=25^\circ\text{C}$ unless otherwise noted)

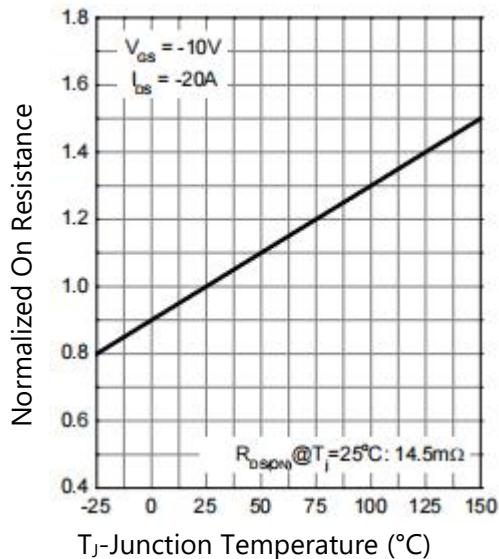
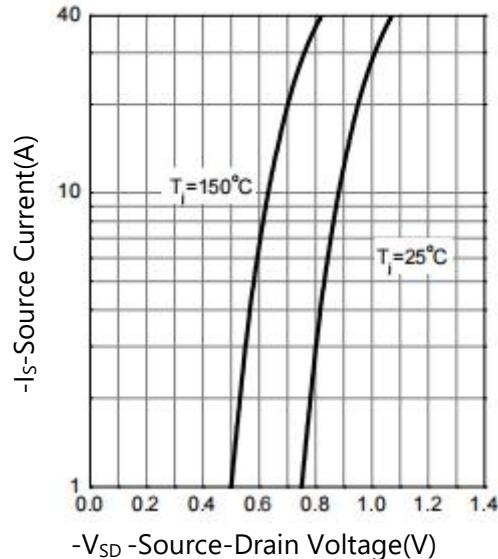
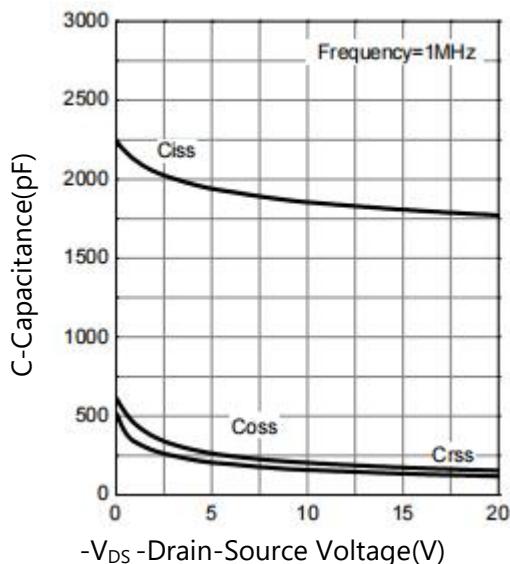
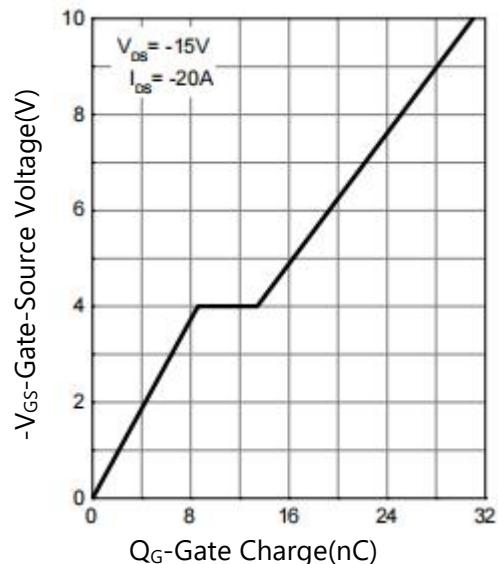
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=-24\text{V}, V_{\text{GS}}=0\text{V}$	-	-	-1	μA
		$V_{\text{DS}}=-24\text{V}, V_{\text{GS}}=0\text{V}, T_J=85^\circ\text{C}$	-	-	-30	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}, V_{\text{DS}}=0\text{V}$	-	-	± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-1.0	-	-2.0	V
Drain-Source On-State Resistance ^(Note1)	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=-4.5\text{V}, I_{\text{D}}=-5\text{A}$	-	24	28	$\text{m}\Omega$
		$V_{\text{GS}}=-10\text{V}, I_{\text{D}}=-8\text{A}$	-	14.5	18	$\text{m}\Omega$
Dynamic Characteristics ^(Note2)						
Input Capacitance	C_{iss}	$V_{\text{DS}}=-15\text{V}, V_{\text{GS}}=0\text{V}, F=1.0\text{MHz}$	-	1811	-	pF
Output Capacitance	C_{oss}		-	172	-	pF
Reverse Transfer Capacitance	C_{rss}		-	134	-	pF
Switching Characteristics ^(Note2)						
Turn-on Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{DS}}=-15\text{V}, I_{\text{D}}=-8\text{A}, V_{\text{GEN}}=-10\text{V}, R_{\text{G}}=4.5\Omega, R_{\text{L}}=0.75\Omega$	-	18	-	nS
Turn-on Rise Time	t_{r}		-	86	-	nS
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$		-	231	-	nS
Turn-Off Fall Time	t_{f}		-	127	-	nS
Total Gate Charge	Q_{g}	$V_{\text{DS}}=-15\text{V}, I_{\text{DS}}=-8\text{A}, V_{\text{GS}}=-10\text{V}$	-	31	-	nC
Gate-Source Charge	Q_{gs}		-	8.6	-	nC
Gate-Drain Charge	Q_{gd}		-	4.8	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note1)	V_{SD}	$V_{\text{GS}}=0\text{V}, I_{\text{SD}}=-8\text{A}$	-	-	-1.3	V
Reverse Recovery Time	t_{rr}	$I_{\text{SD}}=-8\text{A}, \frac{dI_{\text{SD}}}{dt}=100\text{A}/\mu\text{s}$	-	8.3	-	nS
Reverse Recovery Charge	Q_{rr}		-	0.6	-	nC

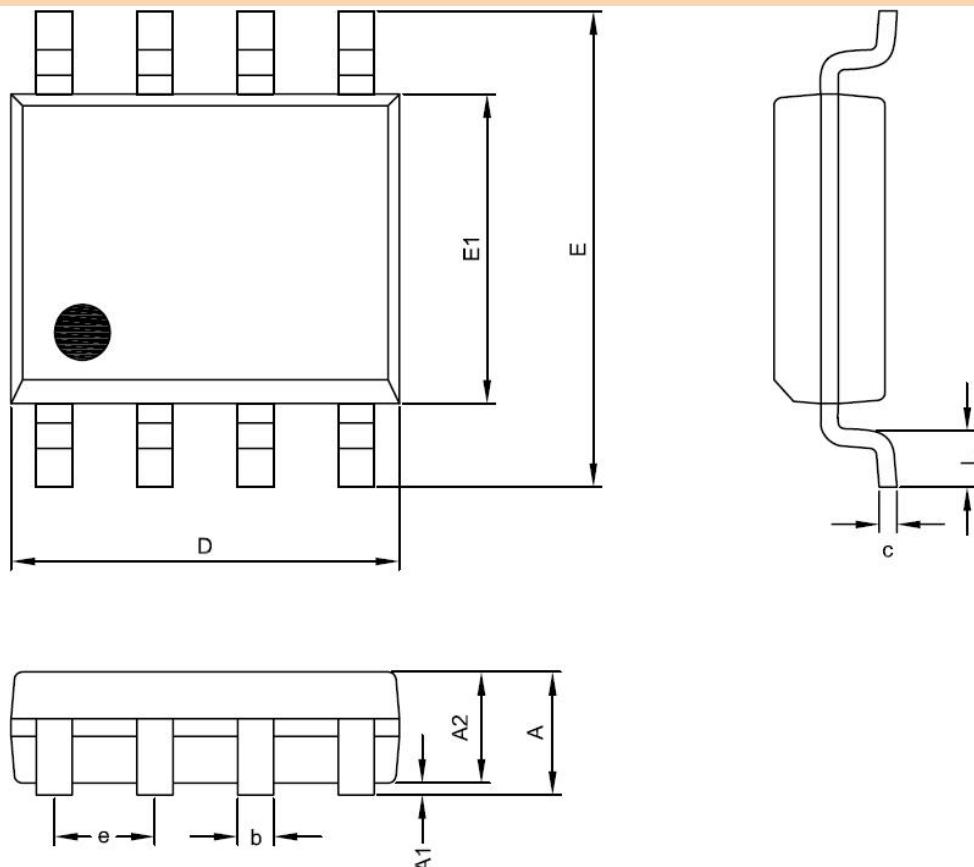
Note 1. The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

Note 2. Guaranteed by design, not subject to production testing


TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
Figure 1. Power Capability

Figure 2. Current Capability

Figure 3. Safe Operation Area

Figure 4. Transient Thermal Impedance



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
Figure 5. Output Characteristics

Figure 6. Drain-Source On Resistance

Figure 7. Transfer Characteristics

Figure 8. Normalized Threshold Voltage



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
Figure 9. Normalized On Resistance

Figure 10. Diode Forward Current

Figure 11. Capacitance

Figure 12. Gate Charge


PACKAGE INFORMATION
SOP-8L


Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	1.35	1.75
A1	0.00	0.25
A2	1.15	1.50
D	4.80	5.00
E	5.80	6.20
E1	3.80	4.00
c	0.19	0.27
b	0.33	0.53
e	1.27 BSC	
L	0.40	1.27

Notes:

1.Jedec outline : MS-012AA

2.Dimensions " D " does not include mold flash, protrusions and gate burrs shall not exceed .15 mm (.006 in) per side .

3.Dimensions " E1 " does not include inter-lead flash, or protrusions. Inter-lead flash and protrusions shall not exceed .25 mm (.010 in) per side.