

## DESCRIPTION

The MXT015N10TAL uses advanced trench technology to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

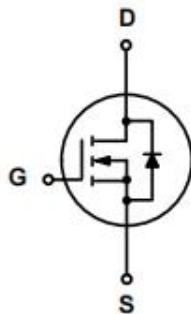
## GENERAL FEATURES

- $V_{DS}=100V$ ,  $I_D=500A$
- $R_{DS(ON)}(\text{Typ.})=1.4m\Omega$  @  $V_{GS}=10V$
- Advanced trench cell design
- Super-mounted package
- Super Trench

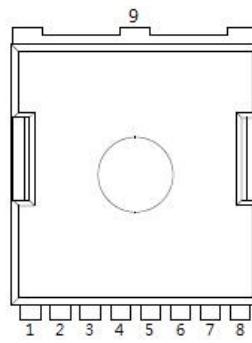
## APPLICATION

- Power Tool appliances
- High power inverter system
- BMS appliances

## PINOUT



Schematic diagram



TOLL-8L top view

Pin	Description
1	Gate(G)
2,3,4,5,6,7,8	Source(S)
9	Drain(D)

## ORDERING INFORMATION

Part Number	Storage Temperature	Package	Devices Per Reel
MXT015N10TAL	-55°C to 175°C	TOLL-8L	2000

## ABSOLUTE MAXIMUM RATINGS ( $T_c=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current( $V_{GS}=10V$ ) <sup>(Note3)</sup>	$I_D$	500	A
Drain Current( $T_c=100^\circ C$ , $V_{GS}=10V$ ) <sup>(Note3)</sup>	$I_D$	367	A
Pulsed Drain Current( $V_{GS}=10V$ ) <sup>(Note1)(Note3)</sup>	$I_{DM}$	1200	A
Diode Forward Current	$I_S$	500	A
Drain Power Dissipation	$P_{tot}$	500	W
Operating Junction and Storage Temperature Range	$T_J$ , $T_{STG}$	-55 to 175	°C
Single Pulsed Avalanche Energy	$E_{AS}$	2900	mJ
Thermal Resistance, Junction-to-Ambient <sup>(Note2)</sup>	$R_{\theta JA}$	40	°C/W
Thermal Resistance, Junction-to-Case <sup>(Note2)</sup>	$R_{\theta JC}$	0.25	°C/W

Note 1. Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$

Note 2. Surface Mounted on minimum footprint pad area

Note 3. Limited by bonding wire


**ELECTRICAL CHARACTERISTICS**( $T_A=25^\circ C$  unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	-	4.0	V
On-State Resistance <sup>(Note1)</sup>	$R_{DS(ON)}$	$V_{GS}=10V, I_{DS}=50A$	-	1.4	1.6	$m\Omega$
<b>Dynamic Characteristics</b> <sup>(Note2)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	11260	-	pF
Output Capacitance	$C_{oss}$		-	1715	-	pF
Reverse Transfer Capacitance	$C_{rss}$		-	328	-	pF
<b>Switching Characteristics</b> <sup>(Note2)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DS}=50V, I_{DS}=50A,$ $V_{GEN}=10V,$ $R_G=4.5\Omega, R_L=1\Omega,$	-	34	-	nS
Turn-on Rise Time	$t_r$		-	26	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	78	-	nS
Turn-Off Fall Time	$t_f$		-	30	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=50V, I_{DS}=50A,$ $V_{GS}=10V$	-	224	-	nC
Gate-Source Charge	$Q_{gs}$		-	80	-	nC
Gate-Drain Charge	$Q_{gd}$		-	38	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note1)</sup>	$V_{SD}$	$V_{GS}=0V, I_{SD}=50A$	-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$I_{DS}=50A, V_{GS}=0V$ $dI_{SD}/dt=100A/\mu s$	-	100	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	280	-	nC

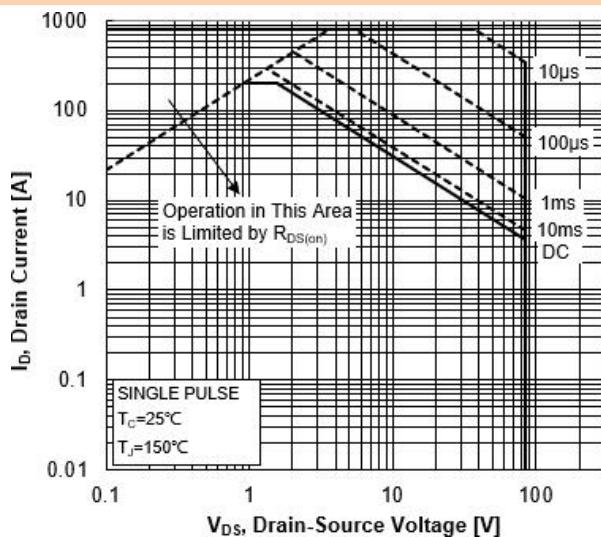
Note 1. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$

Note 2. Guaranteed by design, not subject to production testing

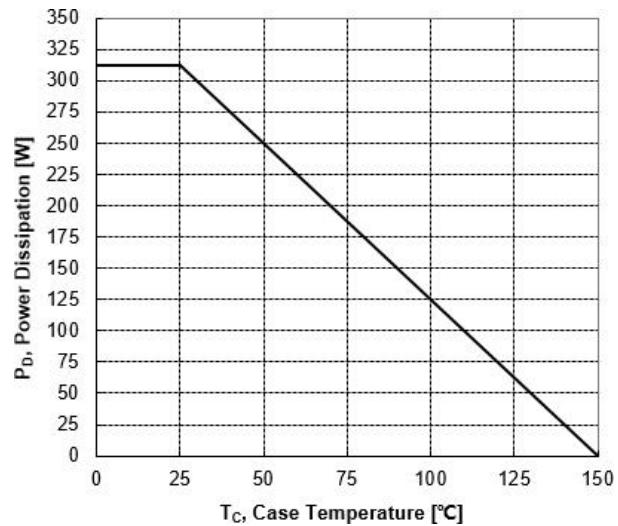


## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

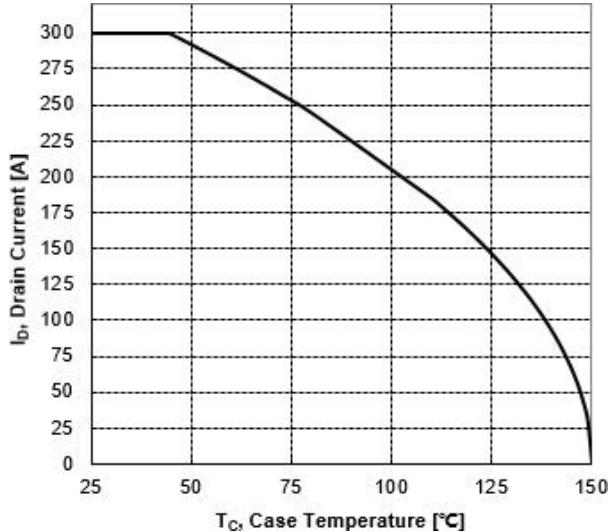
**Figure 1. Safe Operation Area**



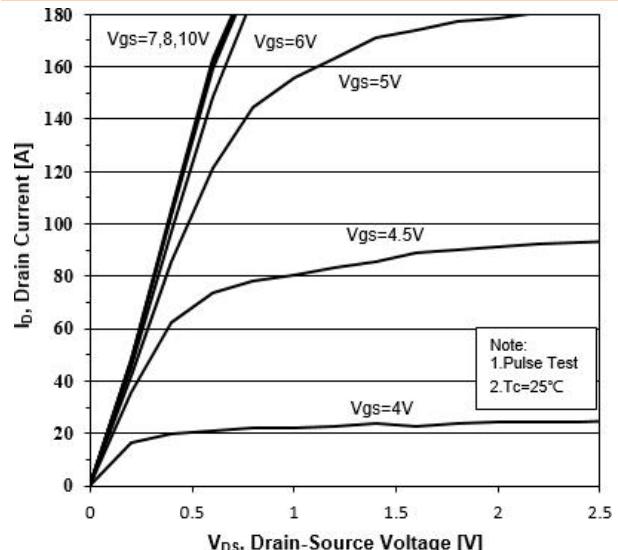
**Figure 2. Maximum Power Dissipation vs Case Temperature**



**Figure 3. Maximum Continuous Drain Current vs Case Temperature**



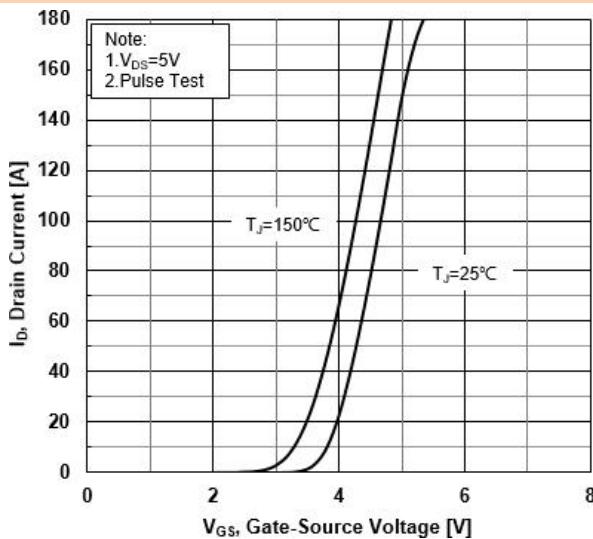
**Figure 4. Typical Output Characteristics**



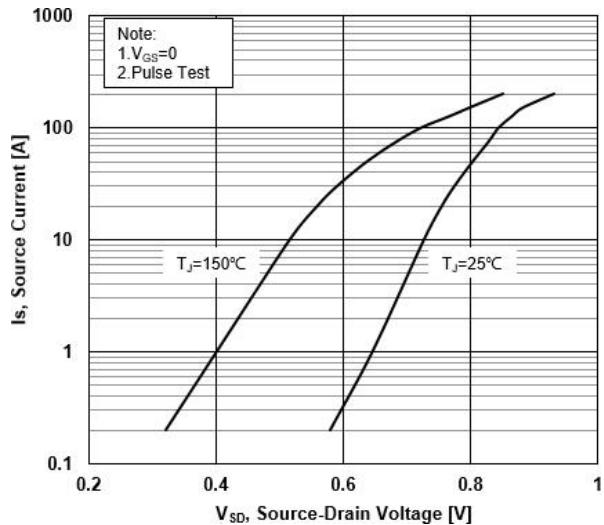


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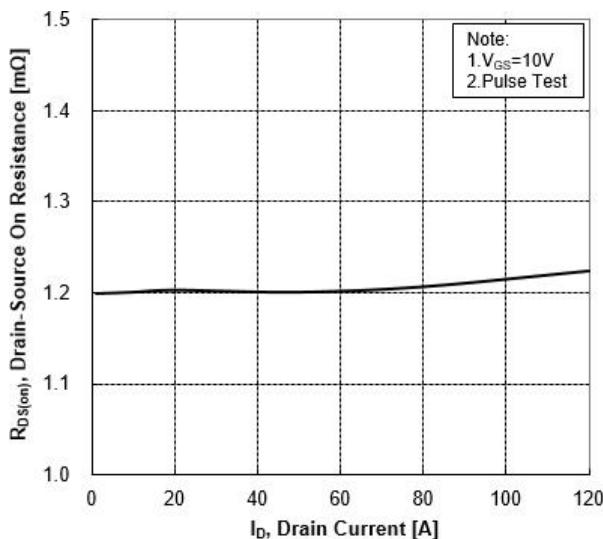
**Figure 5. Typical Transfer Characteristics**



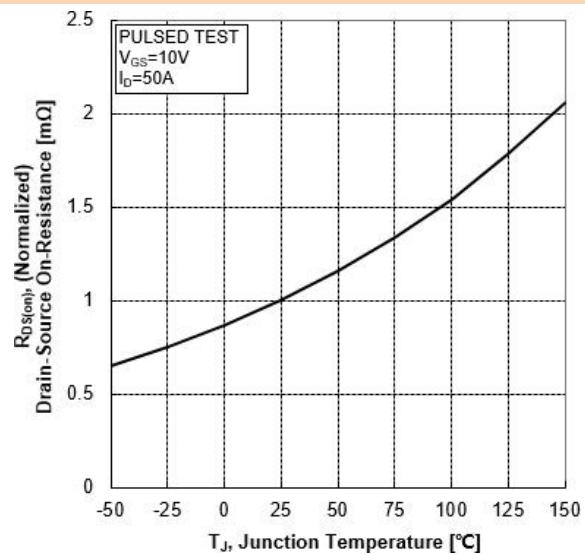
**Figure 6. Source-Drain Diode Forward Characteristics**



**Figure 7. Drain-Source On-Resistance vs Drain Current**



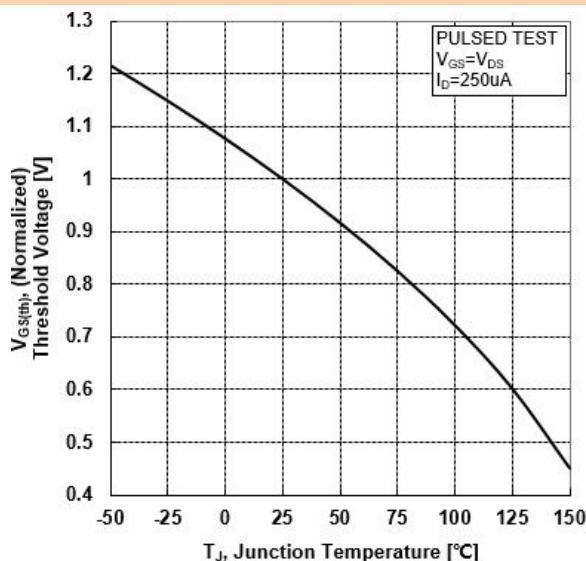
**Figure 8. Normalized On-Resistance vs Junction Temperature**



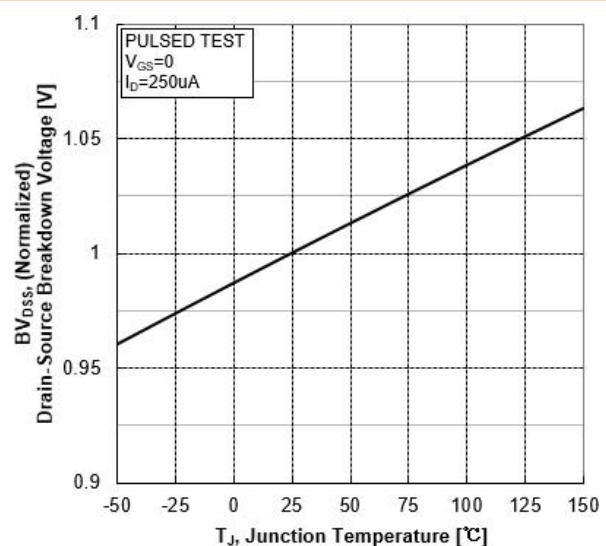


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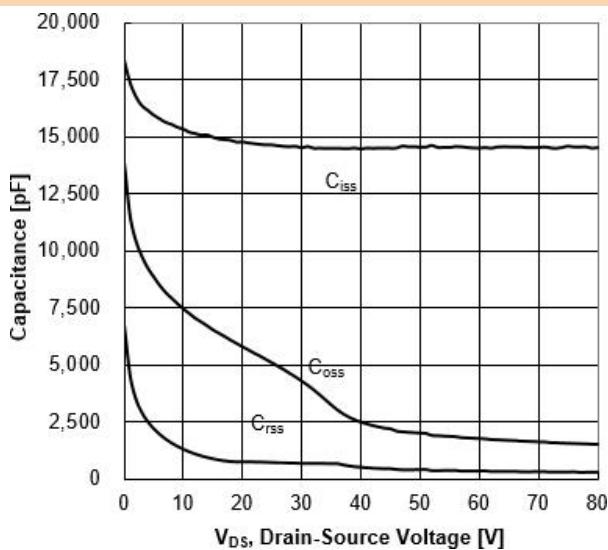
**Figure 9. Normalized Threshold Voltage vs Junction Temperature**



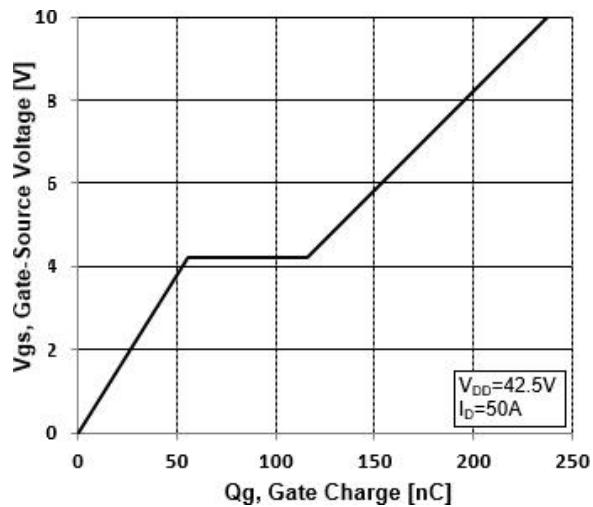
**Figure 10. Normalized Breakdown Voltage vs Junction Temperature**



**Figure 11. Capacitance Characteristics**

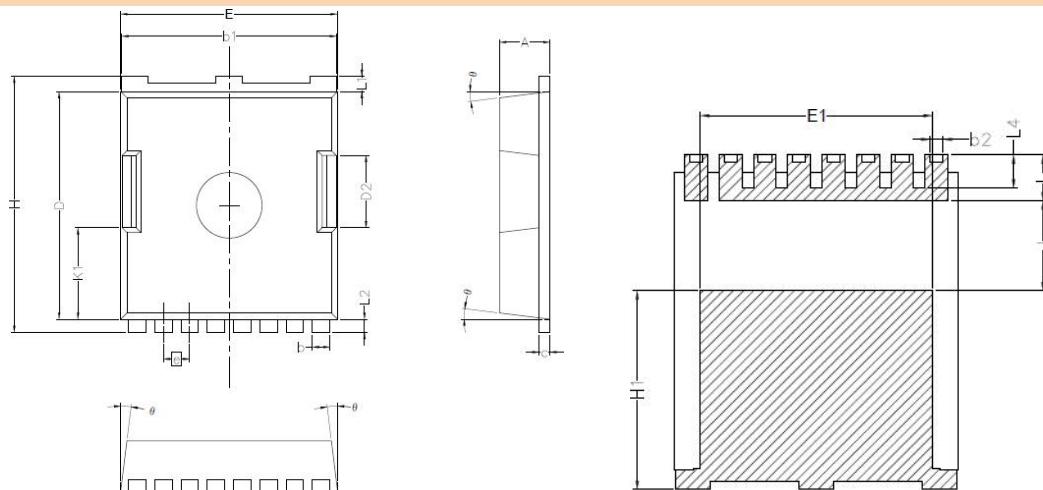


**Figure 12. Typical Gate Charge vs Gate-Source Voltage**



## PACKAGE INFORMATION

### TOLL-8L



Symbol	Dimensions In Millimeters	
	MIN.	MAX.
A	2.20	2.40
b	0.90	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D2	3.10	3.50
E	9.70	10.10
E1	7.90	8.30
e	1.20BSC	
H	11.48	11.88
H1	6.75	7.15
N	8	
J	3.00	3.30
K1	3.98	4.38
L	1.40	1.80
L1	0.60	0.80
L2	0.50	0.70
L4	1.00	1.30
$\theta$	4°	10°